

FIG. 1

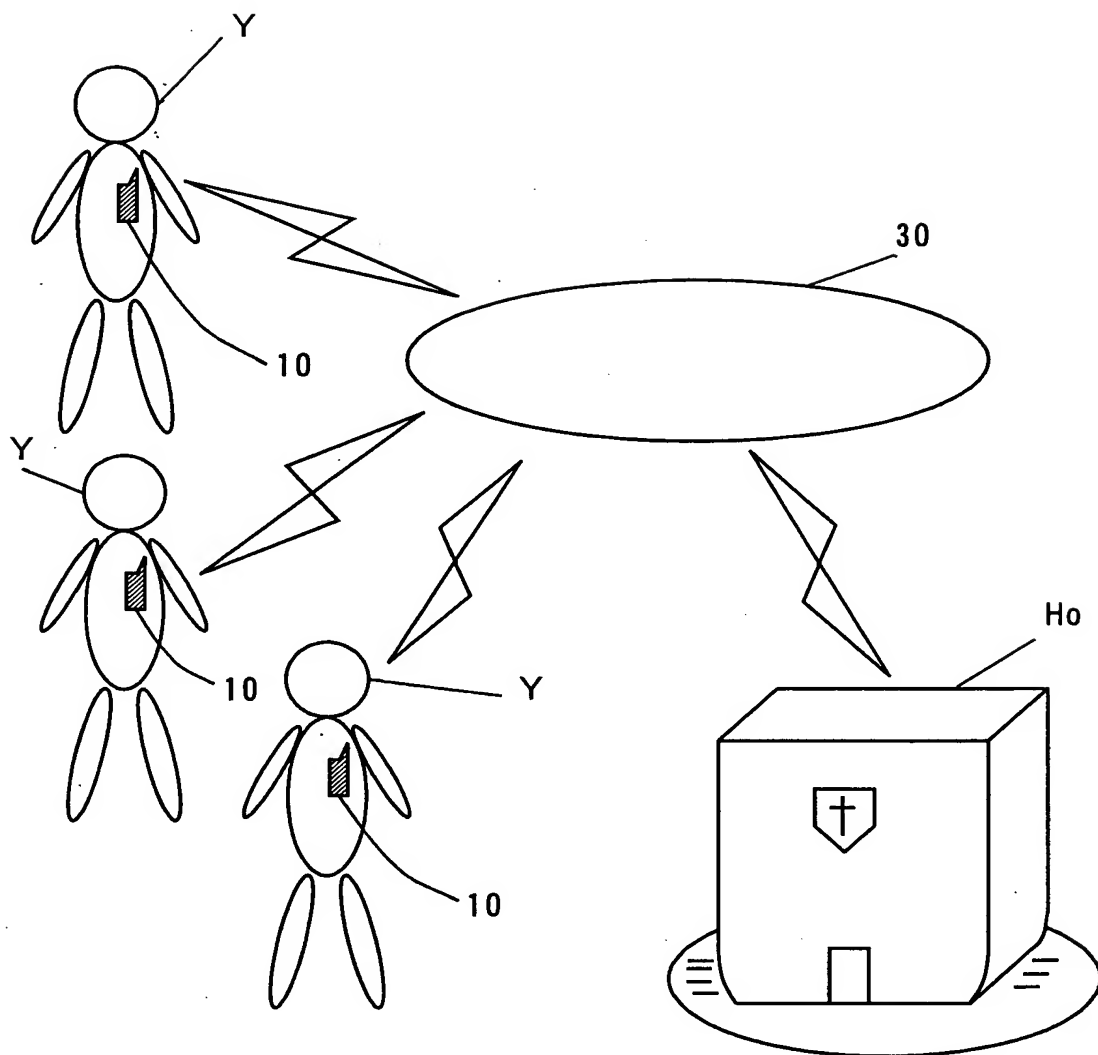


FIG. 2

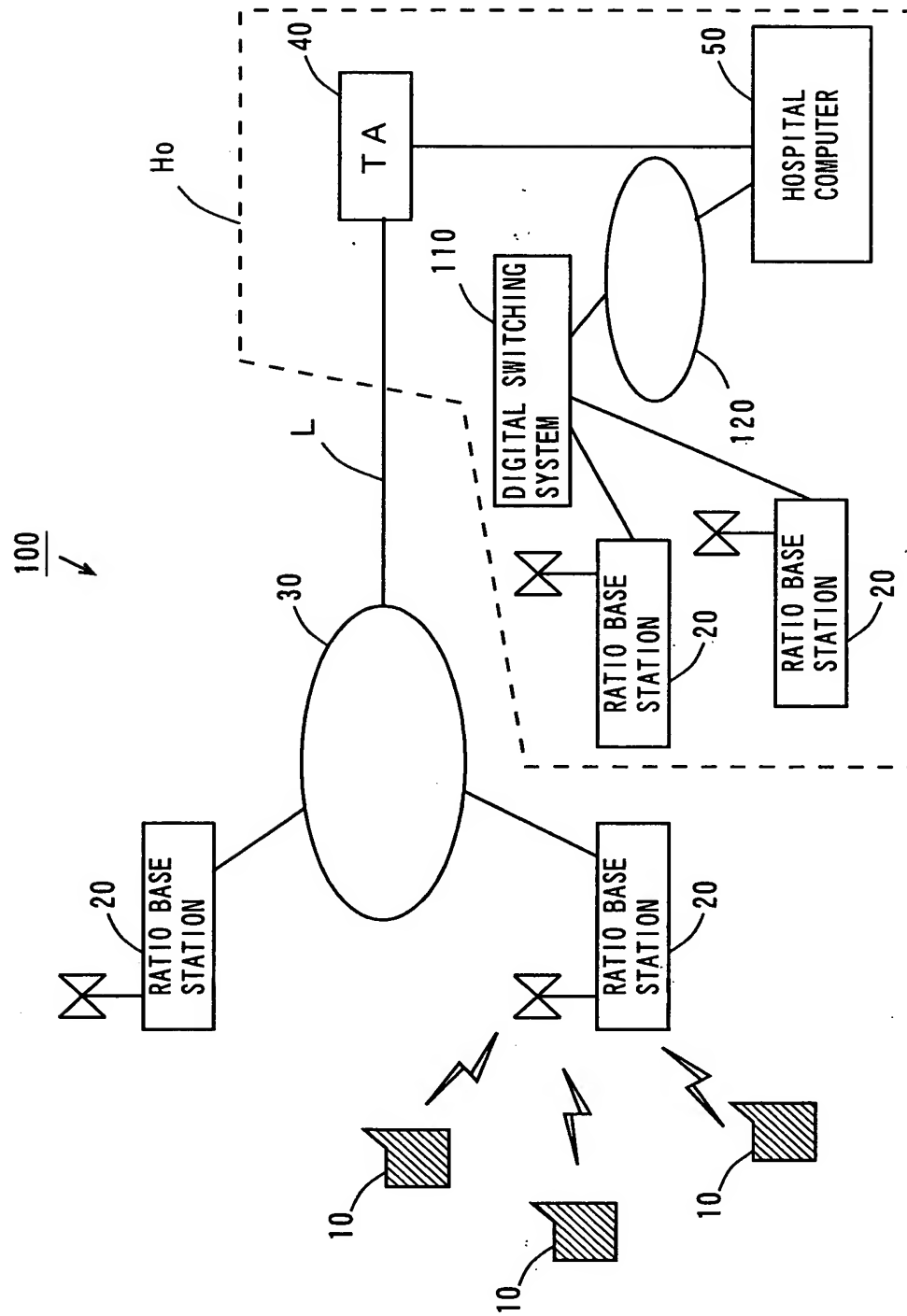


FIG. 3

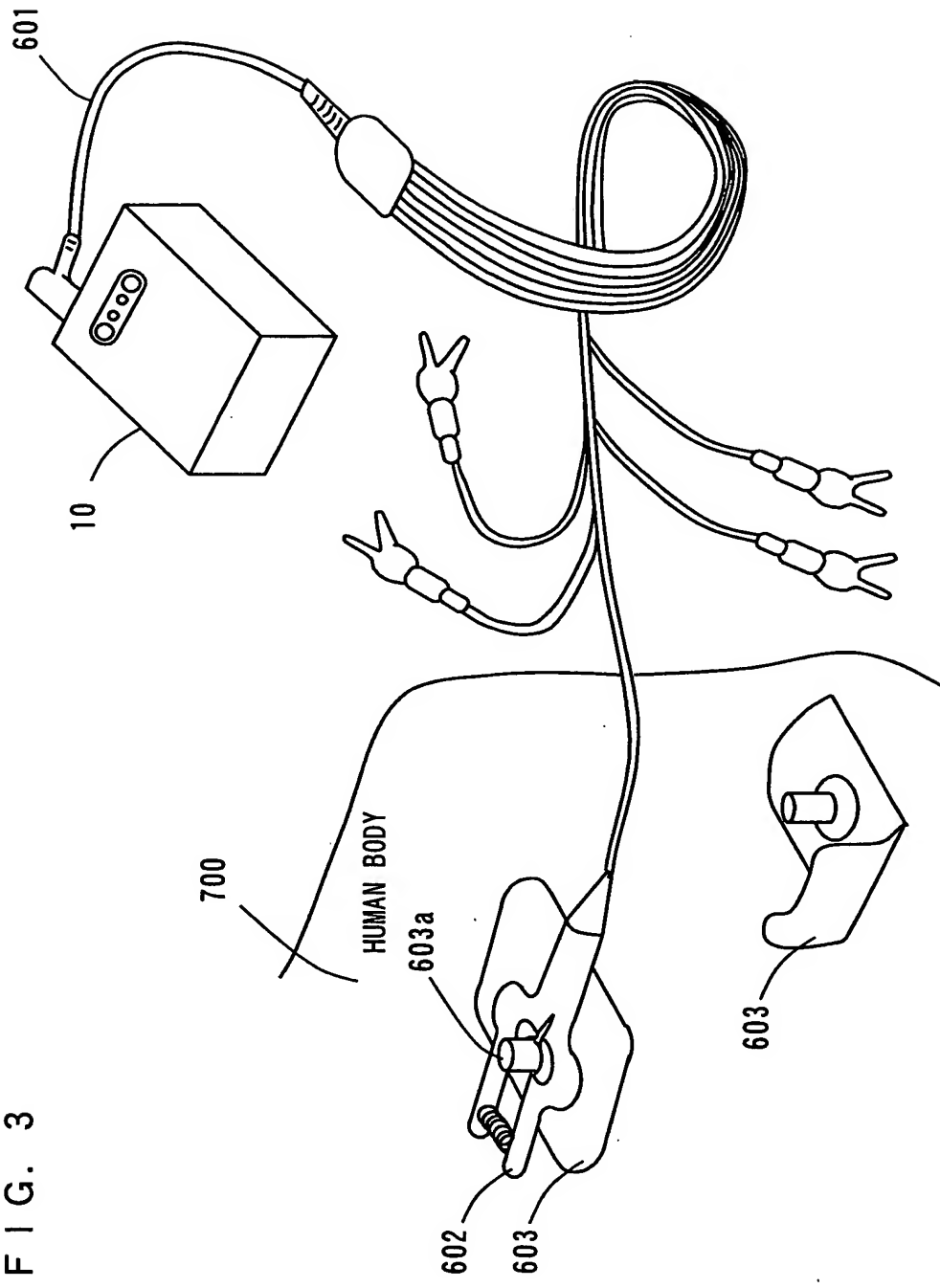
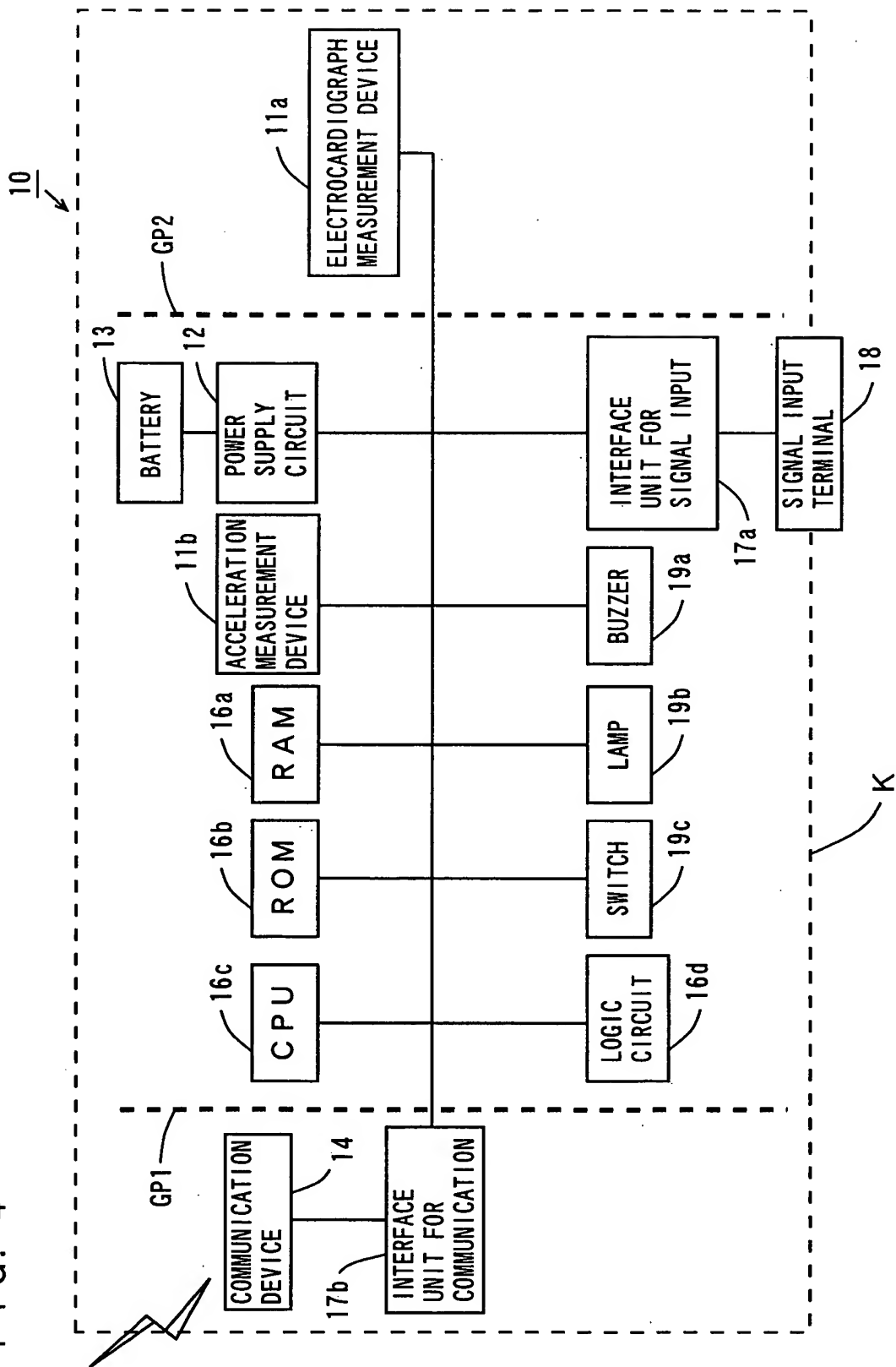


FIG. 4



;

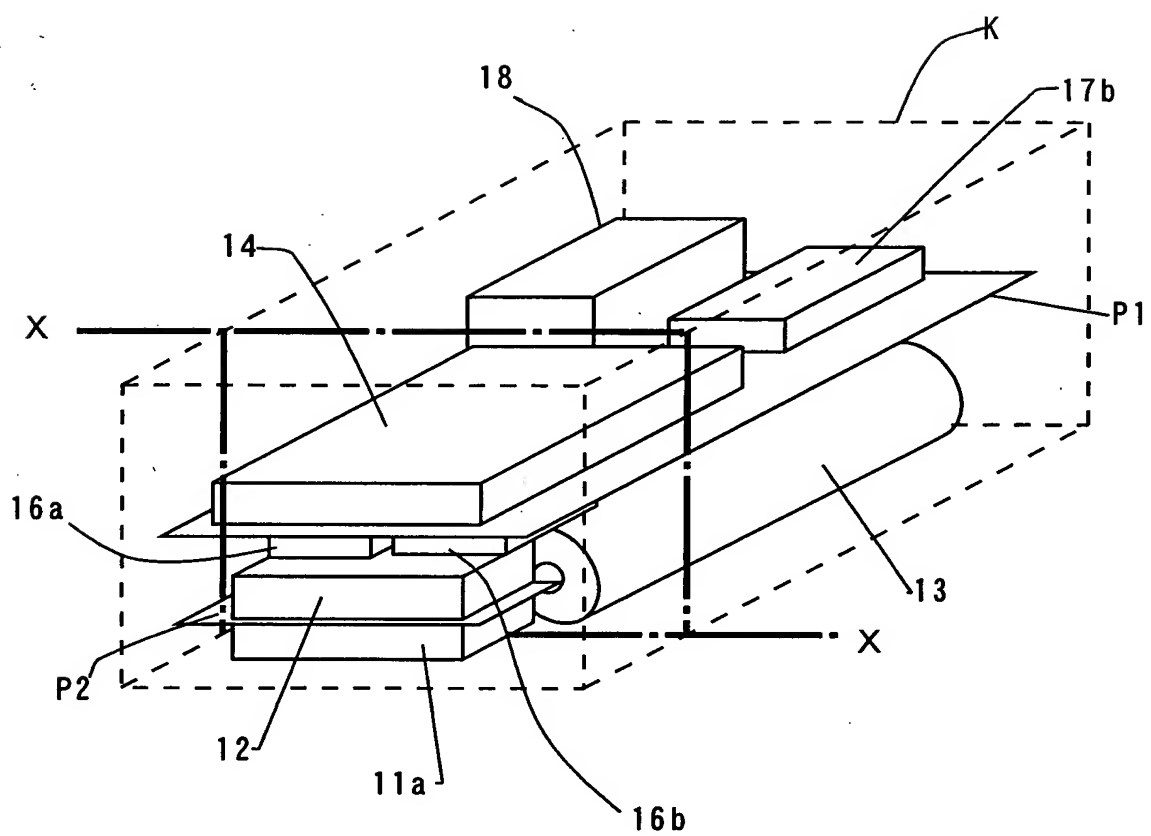
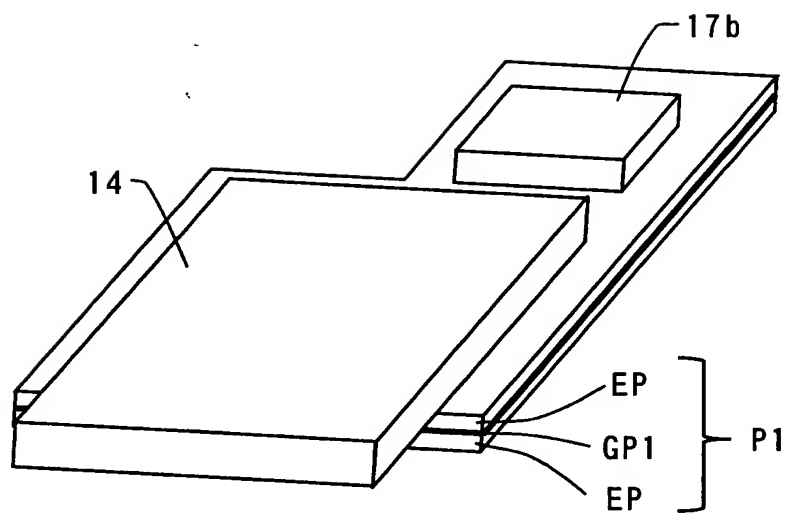


FIG. 6

(a)



(b)

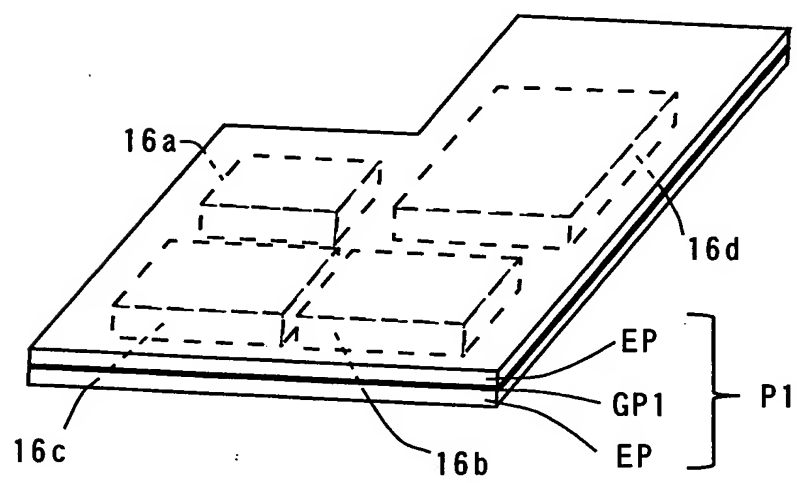


FIG. 7

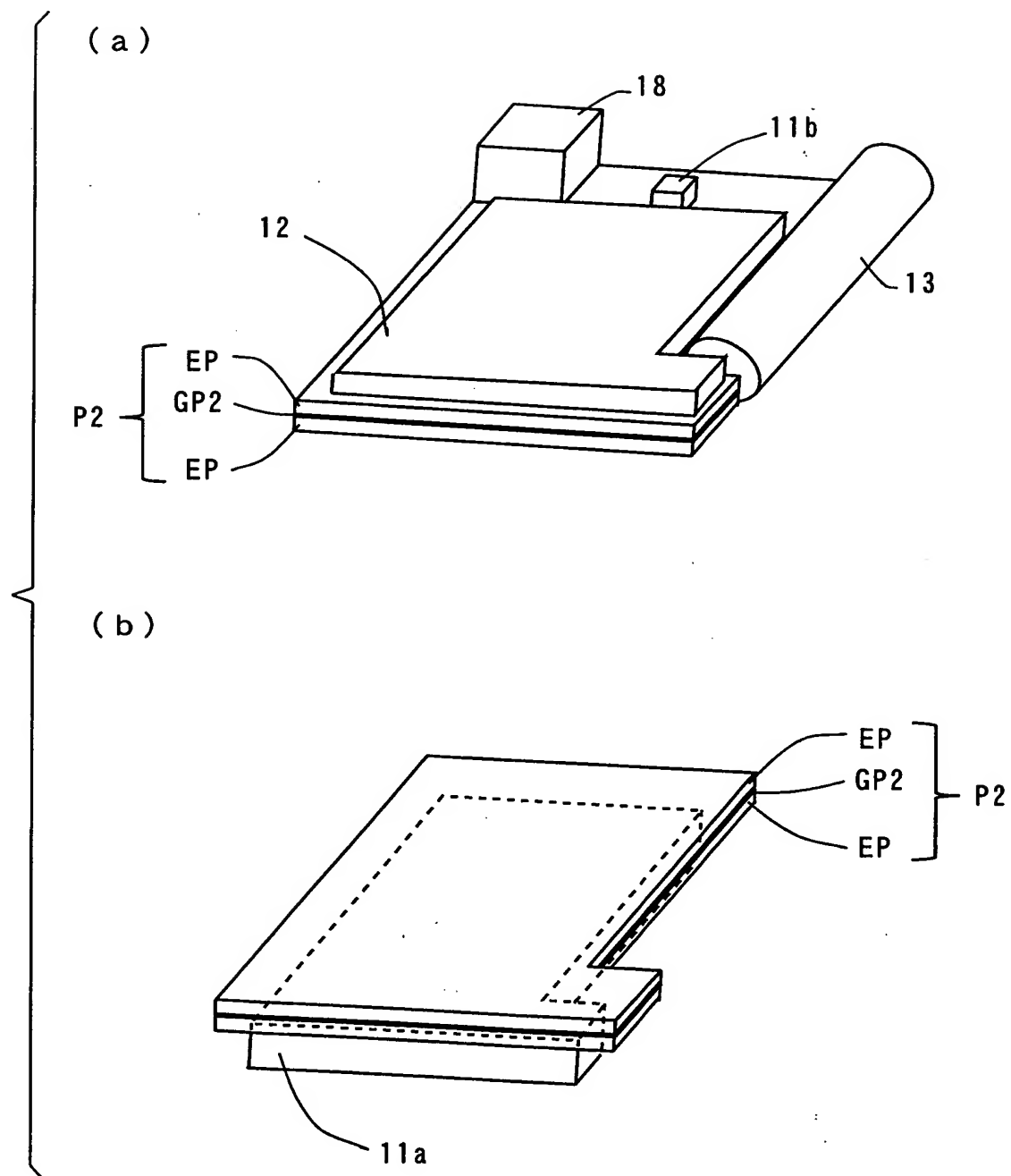


FIG. 8

FIG. 8 is a schematic cross-sectional view of a semiconductor device. The device is enclosed in a rectangular frame 10. Inside, there are two main vertical structures, 11a and 12. Structure 11a is on the left and contains a stack of layers labeled P1, 16a, and 16b. Structure 12 is on the right and contains a stack of layers labeled P2, 16a, and 16b. A circular feature 13 is located between the two structures. Various regions are labeled with 'EP' and 'GP1'. A section line K-K is indicated at the top.

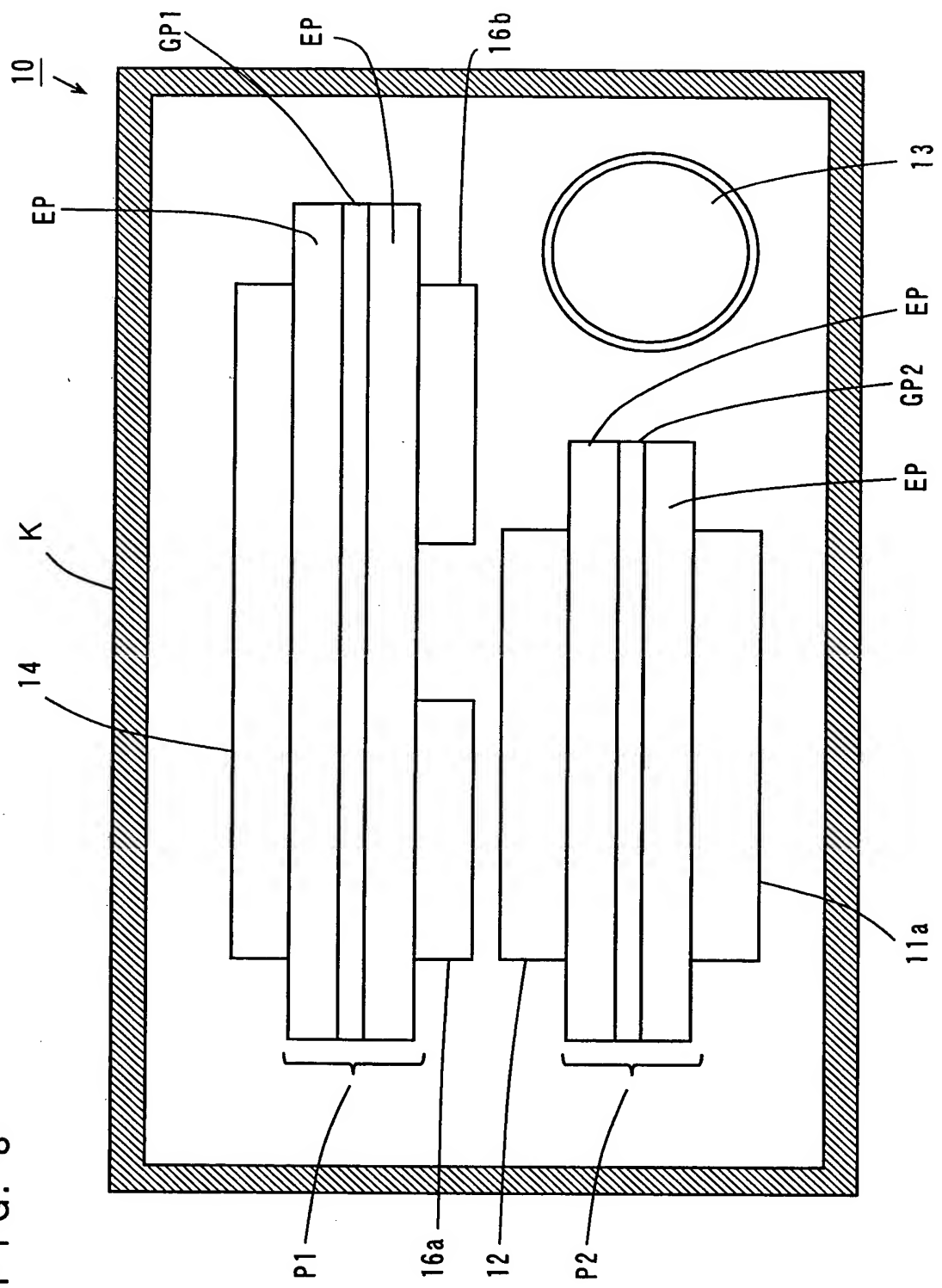




FIG. 9

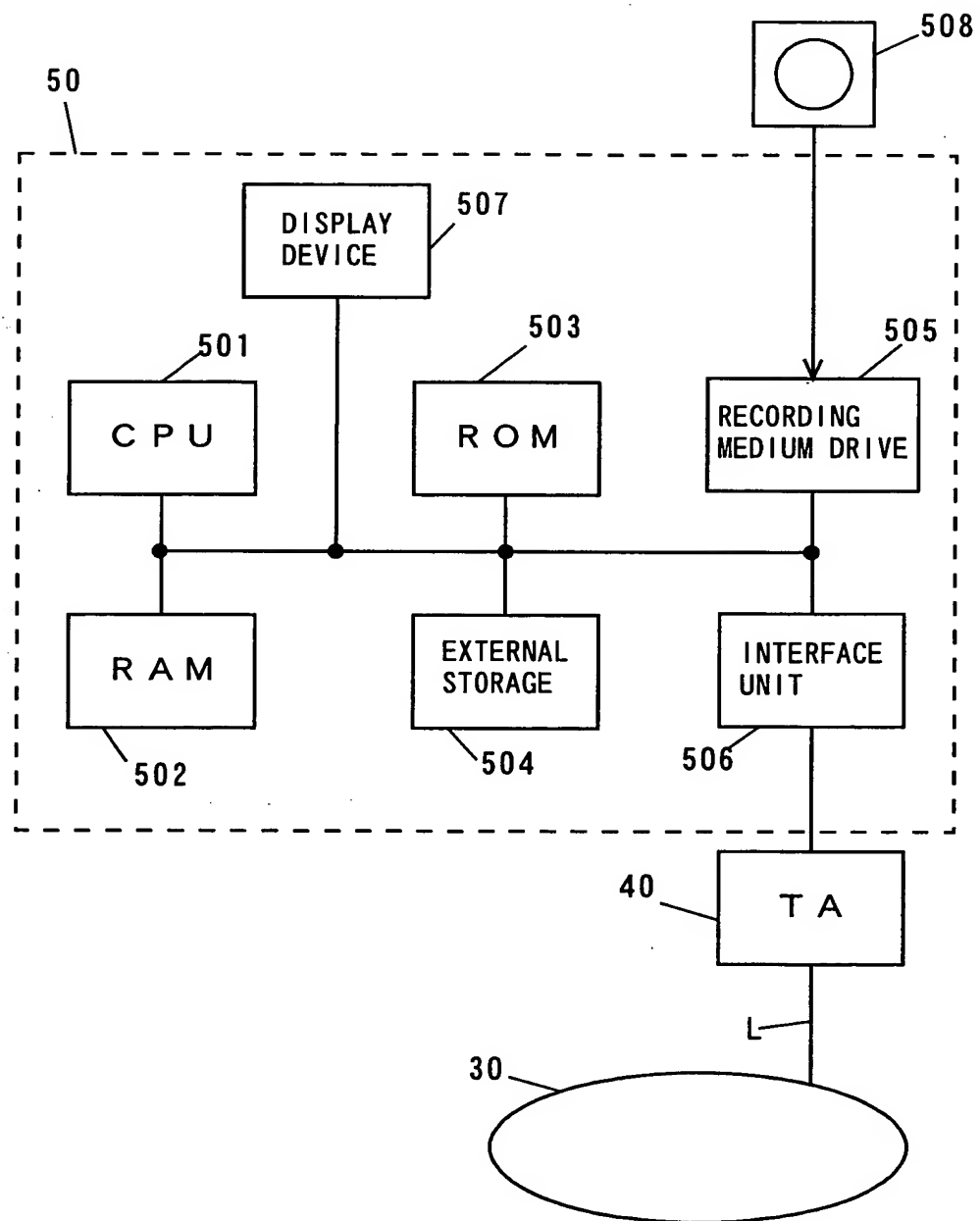


FIG. 10

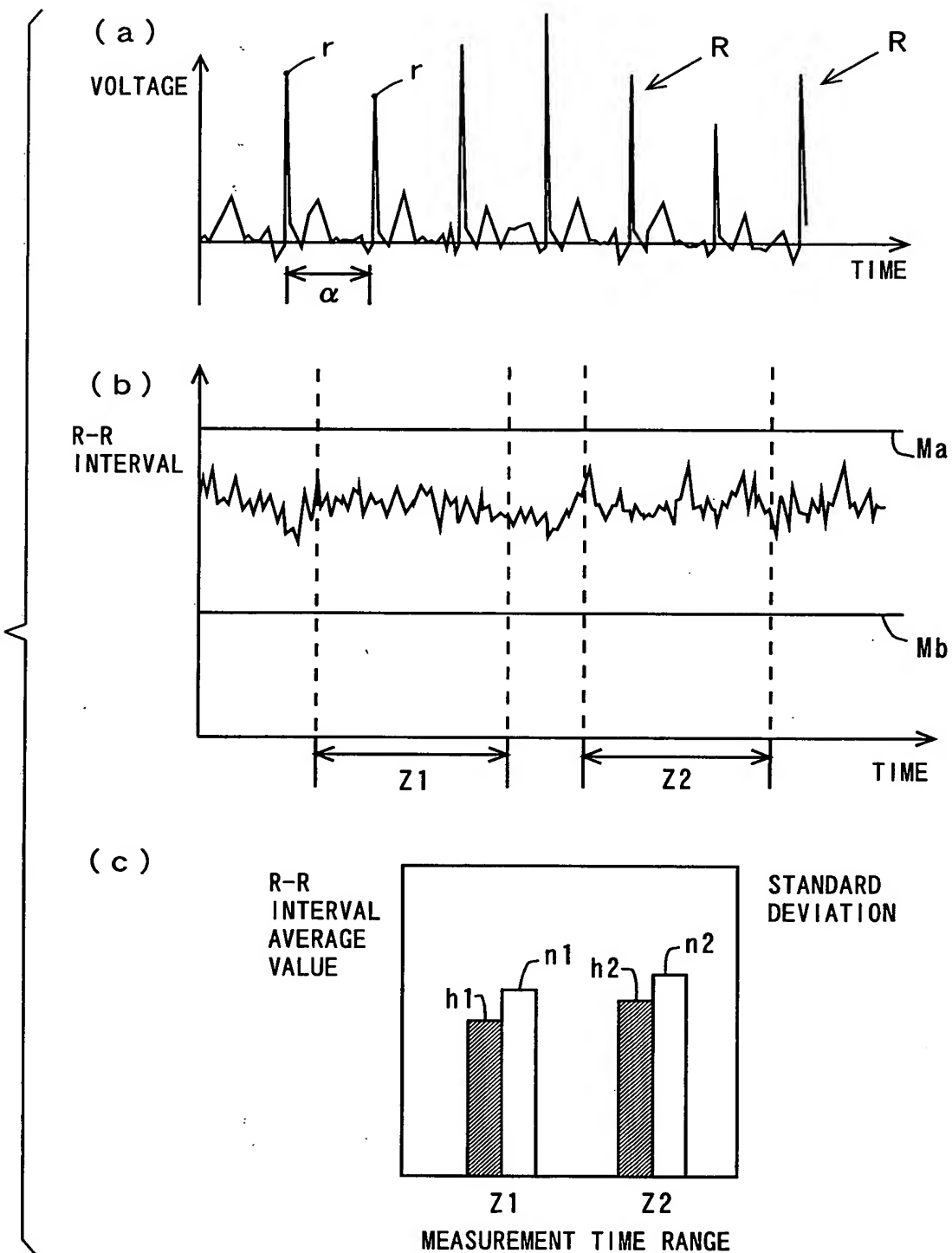


FIG. 11

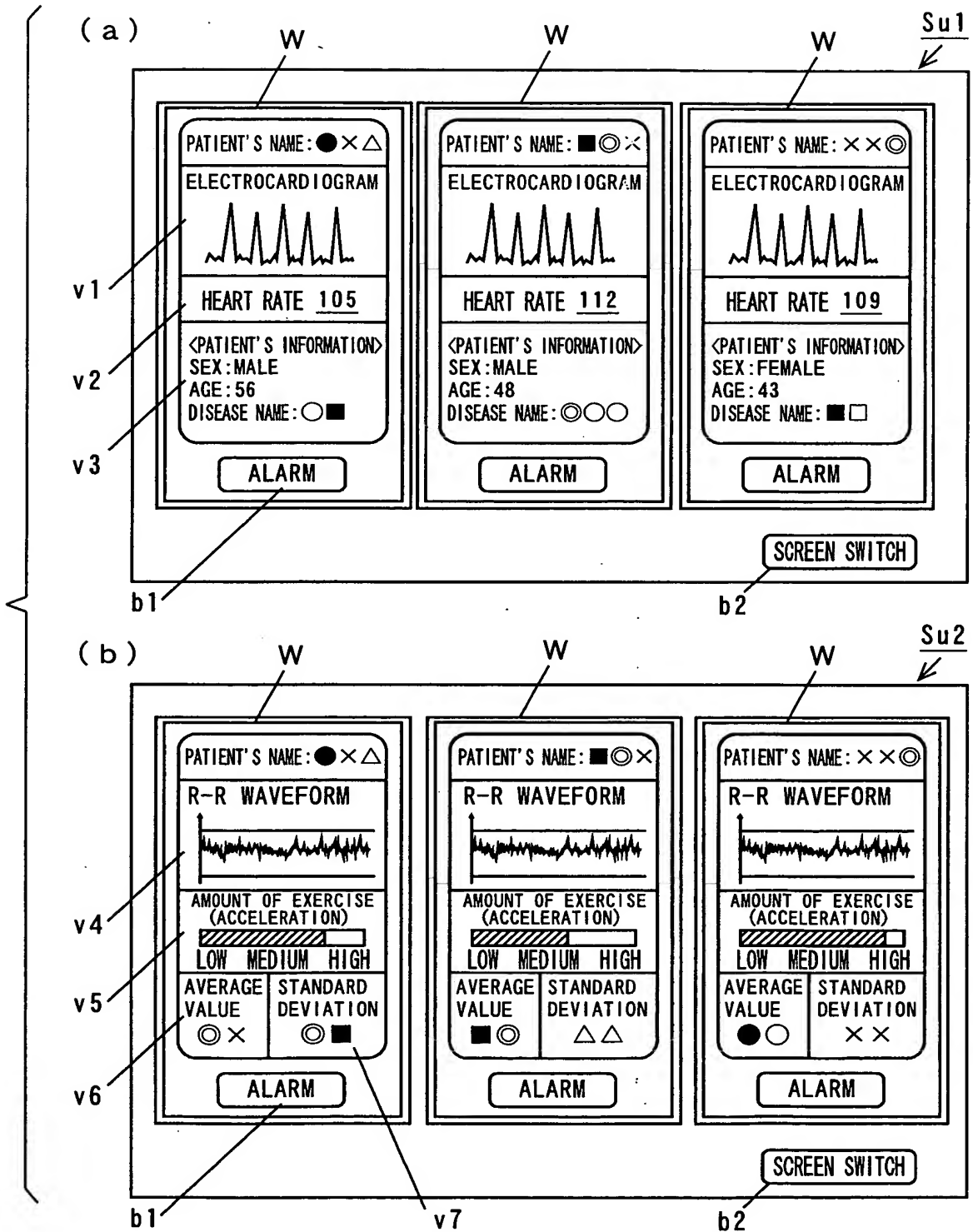


FIG. 12

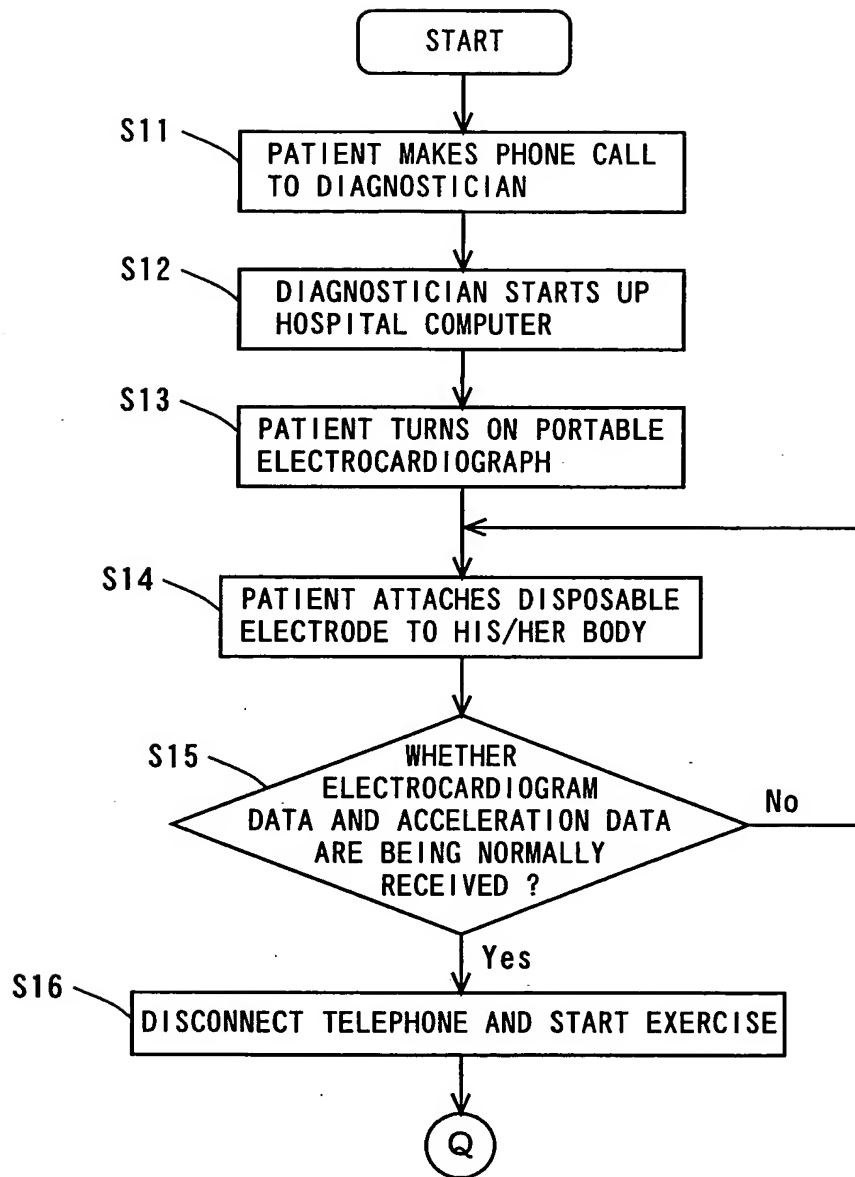


FIG. 13

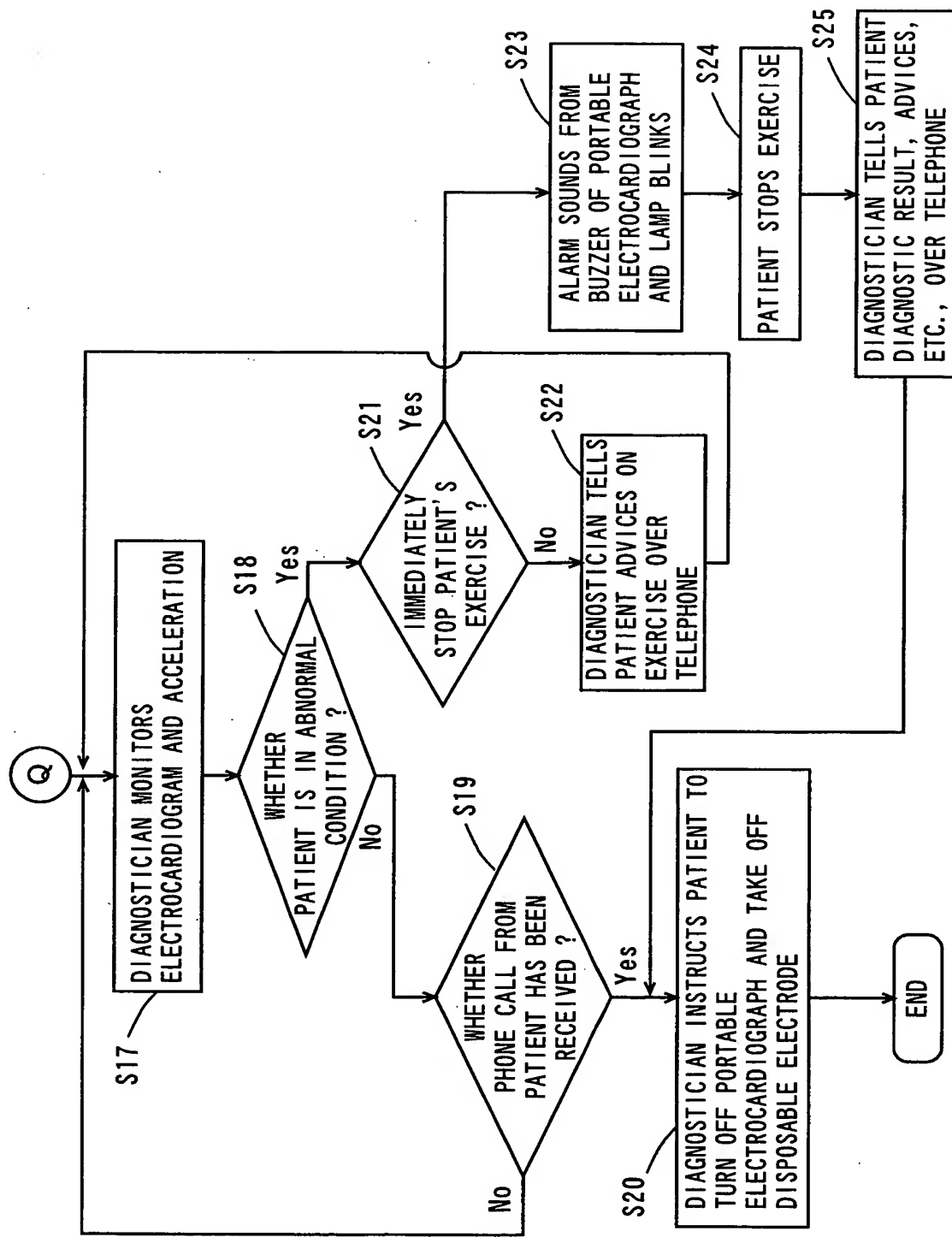


FIG. 14

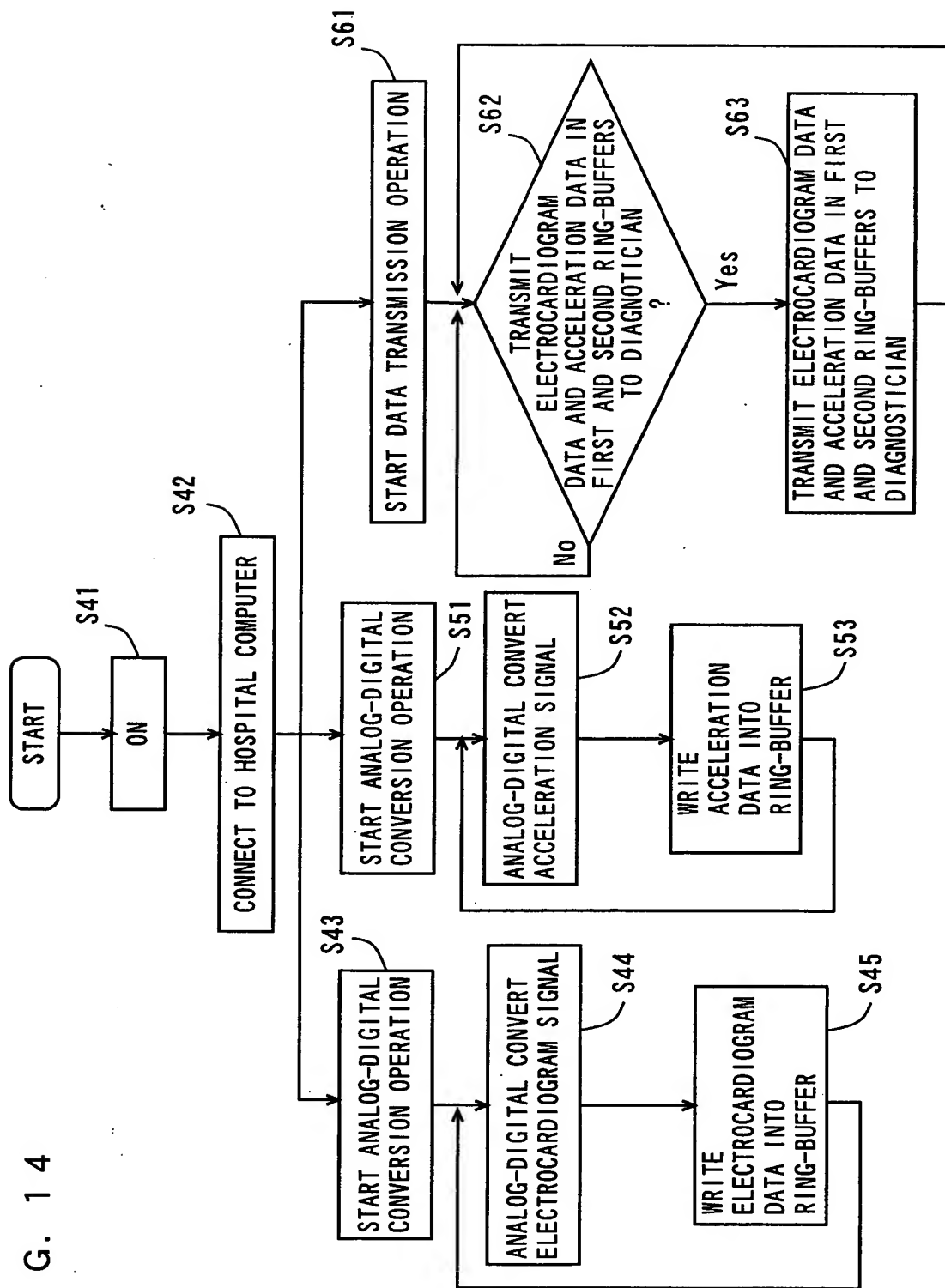


FIG. 15

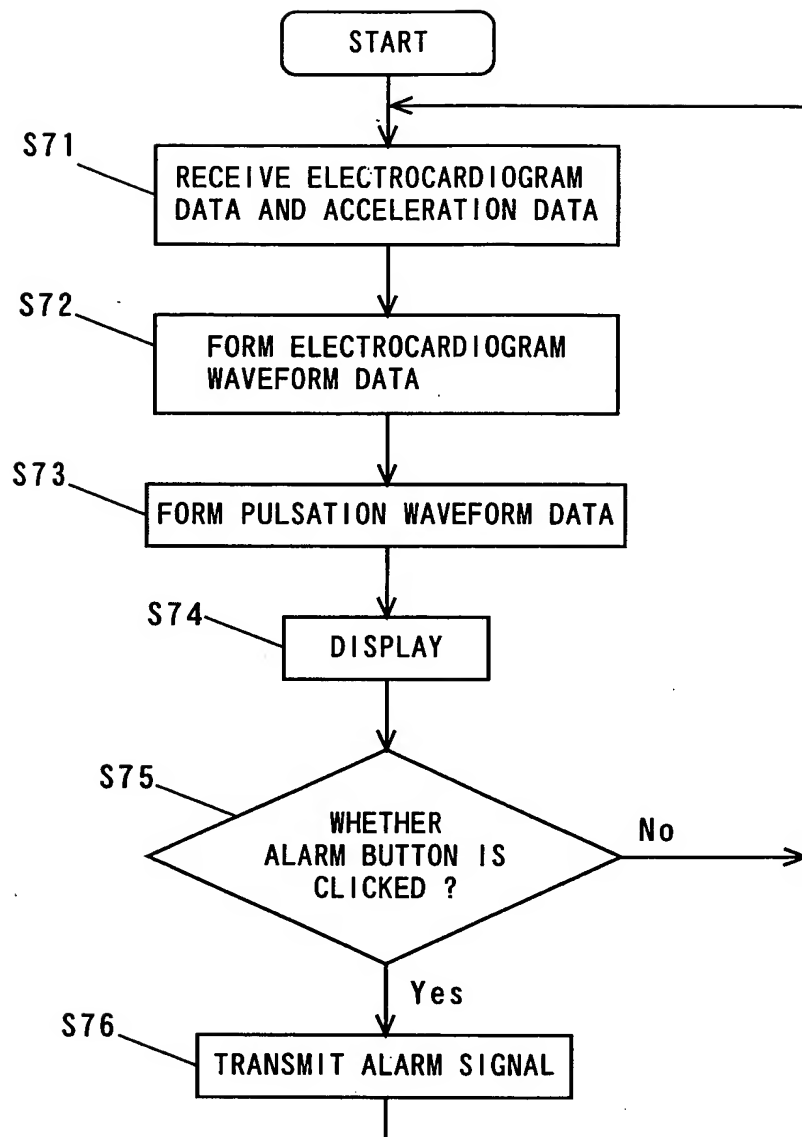


FIG. 16

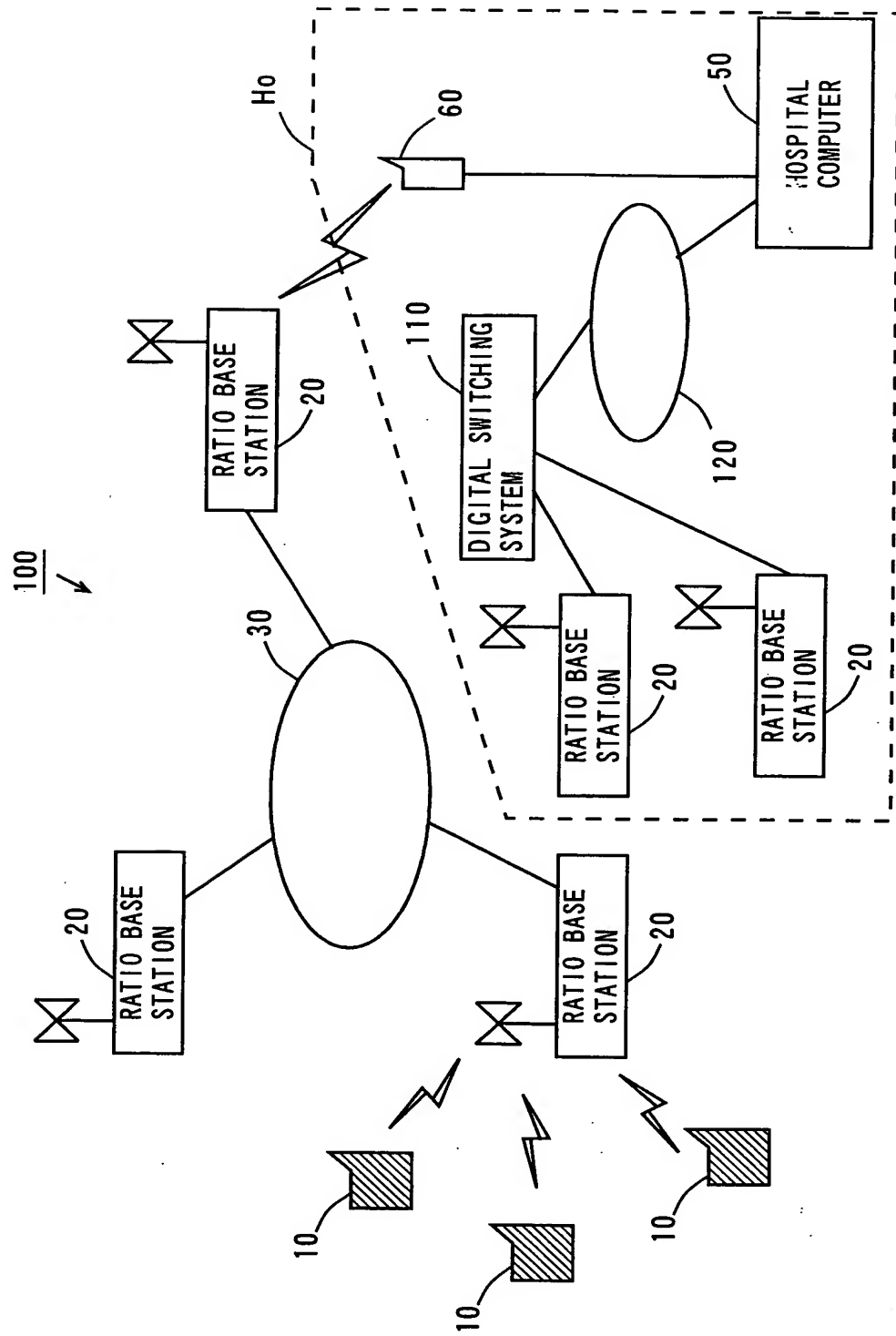




FIG. 17

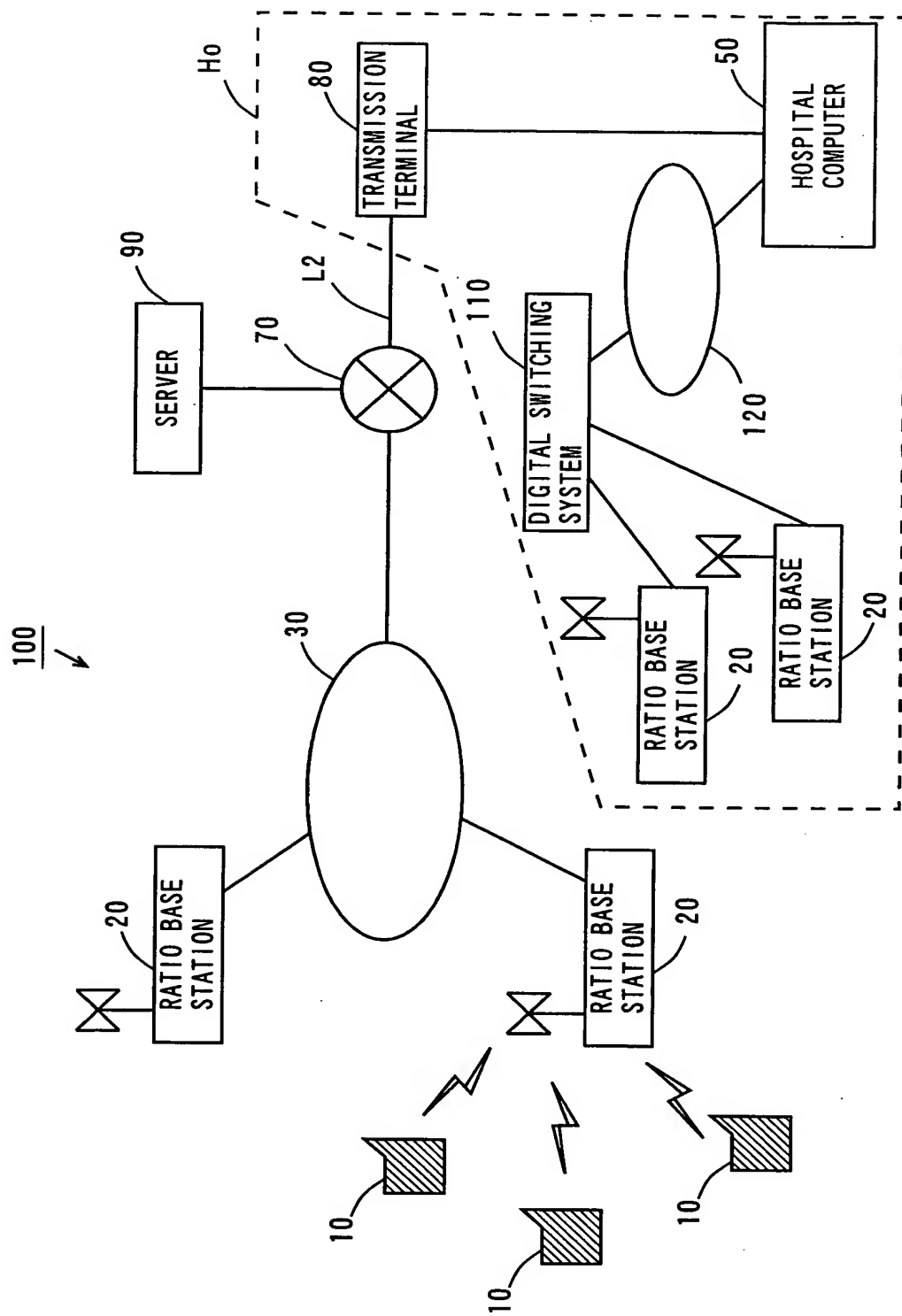


FIG. 18

